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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/618,325	07/11/2003	Hui Jin	Flarion-48APP (84)	4962
26479	7590	08/17/2004	EXAMINER	
STRAUB & POKOTYLO 620 TINTON AVENUE BLDG. B, 2ND FLOOR TINTON FALLS, NJ 07724			BAKER, STEPHEN M	
			ART UNIT	PAPER NUMBER
			2133	
DATE MAILED: 08/17/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/618,325

Applicant(s)

JIN ET AL.

Examiner

Stephen M. Baker

Art Unit

2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-26 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>071103</u> . | 6) <input type="checkbox"/> Other: ____.  |

## **DETAILED ACTION**

### ***Claim Objections***

1. Claims 1, 3, 5, 6, 11 and 12 are objected to because of the following informalities:

In claim 1: in line 7, "passing computed" apparently should be "passing a computed".

In claim 3: in line 3, "the switching of" apparently should be "the switching for".

In claim 5: in lines 2 and 3 (both occurrences), "order of vectors" apparently should be "order the vectors".

In claim 6: in line 1, "claim 2" apparently should be "claim 4", or "the rotation" in line 3 apparently should be "a rotation".

In claim 11: in line 1, "claim 2" apparently should be "claim 4".

In claim 12: in line 2, "device" apparently should be "module".

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 4, 6 and 13-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 4, 6, 13, 17, 24 and 26: in view of the disclosure (p. 7, lines 32-34) it is not clear whether applicant is using "rotation" and "rotated" synonymously with "permutation" and "permuted".

Claim 18 is apparently redundant with claim 19 and so apparently should be deleted.

In claim 24: the reference to "the rotated Z bit vector" in lines 9-10 implies that an essential preceding step of either reading the "rotated" vector or "rotating" the read vector has been omitted.

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-10, 13-15 and 17-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,864,703 to van Hook et al (hereafter van Hook '703) in view of U.S. Patent No. 5,933,650 to van Hook et al (hereafter van Hook '650).

Van Hook '703 discloses a computer system including a co-processor that provides a SIMD vector processing system. A register file (304) of the SIMD vector processing system provides a "memory including a set of memory locations for storing L sets of Z-bit vectors". A SIMD vector unit (302) of the SIMD vector processing system, which includes an accumulator (312) and which is capable of processing an output

instruction (514), provides a “vector unit operation processor including an accumulator and output device for passing (a) computed Z-bit vector to the said memory in response to operation instructions”. A pair of crossbars (314, 316) provide a “switching device coupled to the memory and to the vector unit operation processor, the switching device for passing a Z-bit vector between said memory and said vector unit operation processor in response to switch control information”. Van Hook ‘703 mentions application of the system to multimedia data, but does not specifically describe such applications as including “encoding operations”.

Van Hook ‘650 also discloses a SIMD vector processing system including a SIMD vector unit (316). A crossbar circuit (314) is described in detail. The crossbar circuit’s “switch control information” is in the form of a shuffle instruction. The crossbar is useful in using van Hook’s system to perform DCT transforms, which are “encoding operations” for data compression.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to apply the SIMD vector processing system disclosed by van Hook ‘703 to the DCT transform “encoding operations” mentioned by van Hook ‘650. Such an application would have been obvious because both disclosures apparently pertain to the same type of SIMD vector processing system.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the crossbars (314, 316) shown by van Hook ‘703 in the manner of crossbar (314) circuit detail disclosed by van Hook ‘650. Such an

implementation would have been obvious because both disclosures apparently pertain to the same type of SIMD vector processing system.

Regarding claims 2, 9, 10, 18 and 19, reading and writing control of the register file in van Hook's system presumably requires a register file operation instruction decoder, which serves as an "ordering control module" that is "coupled to said memory for generating read and write indices". The generation of vector processing instructions (502-514) for van Hook's SIMD vector unit presumably requires a SIMD vector unit operation instruction decoder, which serves as an "operation control module coupled to said vector unit operation processor for generating unit operation instructions".

Regarding claim 3, the necessary means in van Hook's system for decoding an instruction for controlling the crossbar circuit is for "generating said switch control information used to control the switching (for) said at least one vector" and can arbitrarily be considered a part of the "ordering control module".

Regarding claims 4, 6 and 17, Fig. 10F of Van Hook '650 shows a "vector rotation operation to generate a rotated vector".

Regarding claims 5, 7 and 8, the necessary instruction storage means in van Hook's system for ordering the sequence of vectors written to, and read from, the register file can be considered a part of the "ordering control module" and a generator of a sequenced pair of "index identifiers" (register file addresses) required to load the SIMD vector unit with two vector operands.

Regarding claim 13, combining two vectors, re-ordered and/or not re-ordered, is presumably a normal operation for the coprocessor, and so would have been an

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obvious operation sequence for van Hook's coprocessor, to a person having ordinary skill in the art at the time the invention was made.

Regarding claims 14, 20 and 23, performing a register file read-modify-write on a vector is presumably a normal operation for the coprocessor, and so would have been an obvious operation sequence for van Hook's coprocessor, to a person having ordinary skill in the art at the time the invention was made .

Regarding claim 15, van Hook discloses that the vector processor unit may perform 'logical' operations, presumably referring to Boolean logic operations, as opposed to 'arithmetic' operations (col. 5, lines 12-14). Van Hook does not specifically mention an XOR operation, however. Official notice is given that the usefulness of XOR functionality in logical operation units was well known at the time the invention was made. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to realize van Hook's vector processor unit with an XOR operation for combining two vectors, re-ordered and/or not re-ordered. Such a realization would have been obvious because the usefulness of XOR functionality in logical operation units was already well known.

Regarding claims 21 and 22, resetting an accumulator after reading the content thereof is presumably a normal operation for the coprocessor, and so would have been an obvious operation sequence for van Hook's coprocessor, to a person having ordinary skill in the art at the time the invention was made.



Regarding claim 24, applying the crossbar (316) re-ordering disclosed by van Hook '703 to the result of the vector processor unit's combining of two vectors, re-ordered and/or not re-ordered, is presumably a normal operation for the coprocessor.

6. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over van Hook '703 in view of van Hook '650 as applied to claim 2 above, and further in view of U.S. Patent No. 6,754,804 to Hudepohl *et al* (hereafter Hudepohl).

Van Hook '703 and '705 do not show an "encoder control module" coupled to the necessary instruction decoders for the register file, the crossbars or the vector processor unit.

Hudepohl discloses a coprocessor interface that is suitable for use with a coprocessor such as disclosed by van Hook '703 and '650 (col. 5, lines 43-46). Hudepohl's coprocessor interface operates to transfer coprocessor instructions to the multiple parallel instruction decoders of the coprocessor, and provides the convenience of supporting various combinations of microprocessor chips and coprocessor chips that otherwise wouldn't work together. When the coprocessor is used for encoding, Hudepohl's interface serves as an "encoder control module".

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the coprocessor interfacing required by van Hook's system by using the coprocessor interface disclosed by Hudepohl. Such an implementation would have been obvious because Hudepohl's coprocessor interface provides the convenience of supporting various combinations of microprocessor chips and coprocessor chips that otherwise wouldn't work together.

***Allowable Subject Matter***

7. Claims 16, 25 and 26 would be allowable if rewritten to overcome the rejections under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

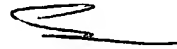
***Conclusion***

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen M. Baker whose telephone number is (703) 305-9681. The examiner can normally be reached on Monday-Friday (11:00 AM - 7:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Stephen M. Baker  
Primary Examiner  
Art Unit 2133

smb